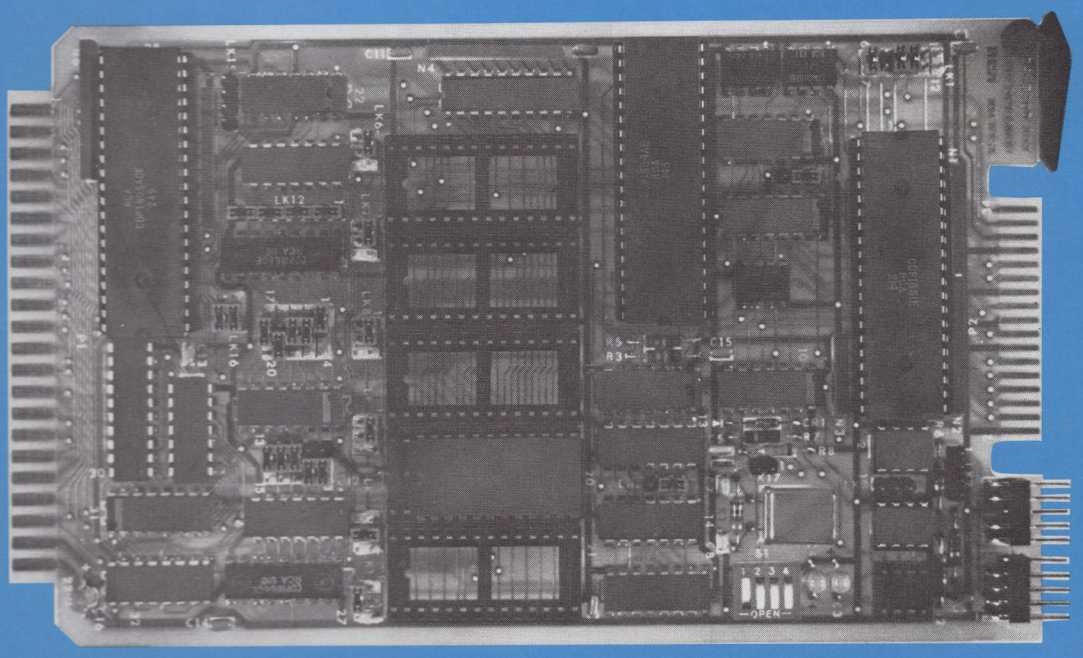
RCA Solid State

RCA CMOS Microboard Computer

CDP18S600



RCA CMOS Microboard
Milliwatt Computer Systems

MB-600

RCA CMOS Microboard Computer

CDP18S600

The RCA Microboard Computer CDP18S600 is a versatile computer system on a single 4.5 x 7.5 inch card. It features a CDP1805A CPU with a powerful expanded instruction set, and can run at up to twice the speed of previous RCA CPU cards. The card contains a complete UART driven RS232 or RS422 serial data link with handshaking, and more than 20 lines of programmable parallel I/O ports. Five memory sockets are provided, one populated with a 2-K byte RAM, allowing a total mix of RAM, EPROM or ROM of up to 40 kilobytes. A crystal controlled oscillator, power-on clear circuitry, and a full Microboard expansion interface complete the board.

The CDP18S600 is a powerful stand alone system, but it may be combined with any of the broad line of Microboard components for larger applications. (Not all Microboards at present will run at the higher of the 2 selectable clock speeds of the CDP18S600; consult RCA.) The CDP18S600 is plug-in compatable with the RCA MSI series of Industrial Chassis and with the RCA Microboard Computer Development Systems (MCDS) CDP18S693 and CDP18S694 and Color CMCDS CDP18S695 to facilitate hardware and software development. It can

Features

- Low power static CMOS — requires 20 mA (typ.)*
- Operable from a single 5 volt supply
- High noise immunity
- 2.46 or 4.92 MHz crystal clock
- Compatible with RCA MSI series Industrial Chassis and 1800-based development systems
- Stand alone capability
- 2 kilobytes of read/write memory — socketed
- Sockets for up to 40 kilobytes of ROM, EPROM, or byte-wide RAM (including socket above)
- Power-on reset
- 1800 series Microprocessor architecture
- Flexible memory and I/O expansion
- 20 programmable parallel I/O lines, plus 4 testable flag inputs and Q output
- 8-bit counter-timer with prescaler
- UART driven serial I/O
- RS232, RS422, or CMOS level serial interface
- 15 selectable BAUD rates: 50 to 38,400
- Addresses full 64 Kbyte memory space
- 44 pin system interface
- Wide temperature range: -40° C to +85° C.
- Small board size: 4.5 x 7.5 inches

*with CMOS ROM and CMOS level serial interface

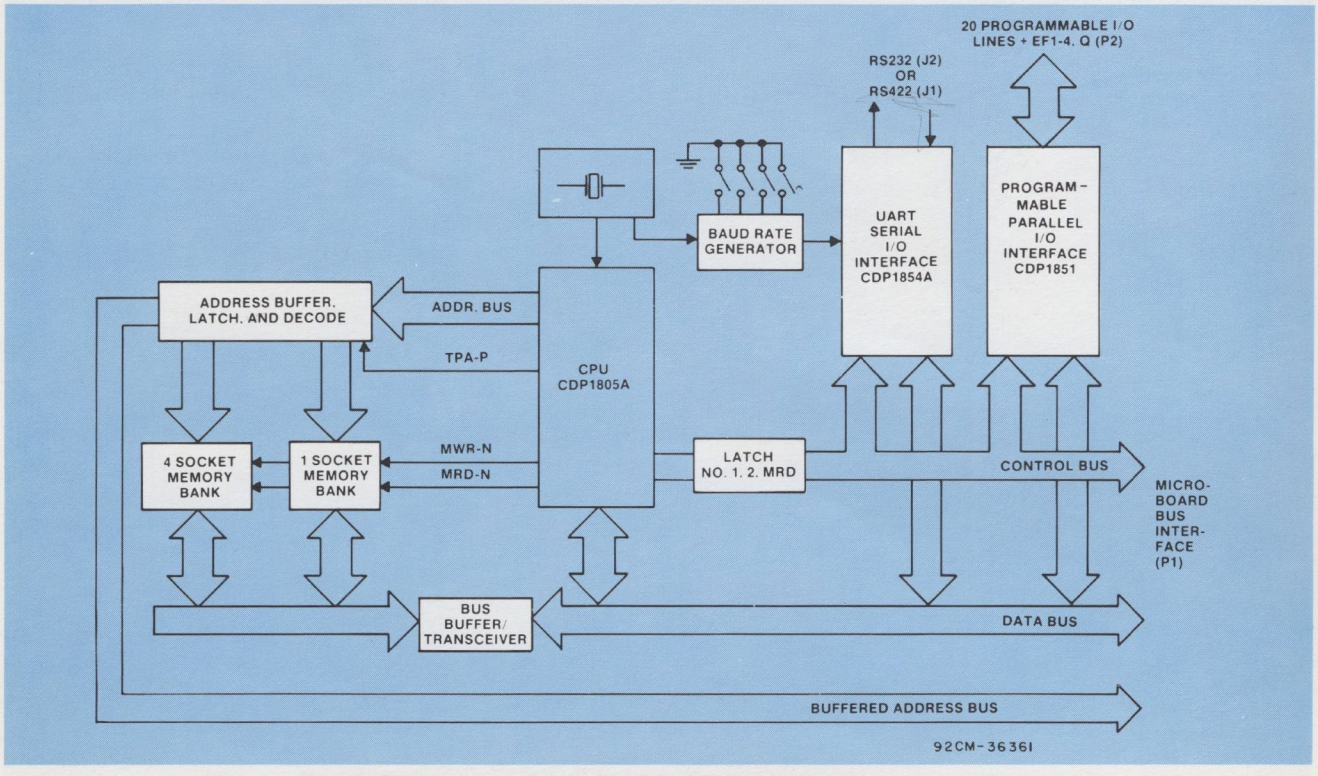


Fig. 1 - Block Diagram of RCA CMOS CDP18S600 Microboard Computer

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also be used with the RCA Development System CDP-18S008 (CDSIV) and the MicroDisk Development System (MS2000).

Because of its CMOS design and low current requirements, the power supply and cooling requirements are minimal. A complete system, including an RS422 data link, could run from a small plug in power supply such as the CDP18S023.

Component Features

Central Processing Unit: The central processor for the CDP18S600 is the 8-bit silicon gate CMOS RCA CDP-1805A. The CDP1805A features 16 general purpose 16-bit registers, any of which can be used as program counter, stack or data pointer, or general data storage. One register serves as a program counter for interrupt servicing, while a second can serve as a DMA pointer for fast I/O transfer of data. If either DMA or Interrupt is unused, its register is free for other uses. A versatile 8-bit counter-timer with prescaler, 4 testable flag lines, a single bit testable output port, and several powerful new instructions are also featured.

Memory: The CDP18S600 provides 2 independent banks, one of 4 sockets and one of one. A 6116 CMOS RAM provided in one of the sockets gives 2 Kbytes of read/ write storage. All 5 sockets may be loaded with 2716 (2K x 8), 2732 (4K x 8), or 2764 (8K x 8) compatible EPROM's or masked ROM's, or 6116 (2K x 8) or 6264 (8K x 8) compatible RAM's.

Serial I/O: A serial communications interface, driven by a CDP1854A UART, has EIA RS232 and RS422 capability. The data format is software selectable, while 15 BAUD rates, from 50 to 38,400, are selectable by a 4-position DIP switch.

Parallel I/O: 20 programmable input or output lines are provided by a CDP1851 programmable parallel I/O port. Each line can be customized to an input or output under software control, while several may be used to provide handshaking for byte transfer applications. The CPU flag and Q lines may also be used as input and output respectively.

Specifications

Memory Capacity

On-board ROM/EPROM/RAM: 5 sockets for up to 40 kilobytes

On-board RAM: 2 kilobytes occupying one of the above sockets

Off-board expansion: Up to 64 kilobytes total memory space

Memory Address Map

On-board RAM: any 2 kilobyte block

On-board ROM/EPROM/RAM: depending on type and quantity of memory, any 2-, 4-, 8-, 16-, or 32-kilobyte block

I/O Capacity

Parallel: 20 lines, each programmable as input or output. 8 of the above are programmable as bidirectional. 4 additional flag inputs and 1 additional bit output.

Serial: Data input and output, and clear to send input and output. Programmable format and switch selectable BAUD rate. RS232, RS422, or CMOS level interface.

Operating Temperature Range

-40° C to +85° C.

Dimensions

4.5 x 7.5 inches (114 x 191 mm)

Board pitch 0.5 inch (12.7 mm) minimum

Power Requirements

(except as noted, 5 volts ± 10%, @ 2.46 or 4.92 MHz)

Without ROM's or serial interface

6 mA in Reset mode (clock independent)

11 or 13 mA in Wait mode, memory access off-board

15 or 23 mA operating all memory access off-board

47 or 53 mA operating every cycle on-board RAM access

With RS422 driver installed (U3)

55 mA additional

With RS232/RS422 receiver installed (U2)

35 mA additional

Optional supplies needed for RS232 driver (U4)

+10 to +15 volts at 8 mA typ.

-5 to -15 volts at 8 mA type.

Connectors

System Interface: Double sided edge fingers, 0.156 inch pitch, 44 conductors

Parallel I/O: Double sided edge fingers, 0.100 inch pitch, 34 conductors

Serial I/O: separate RS422 and RS232 10-pin right angle connectors, 2 row, 0.100 inch spacings (mating headers supplied)

Clock

CPU and Interface: 9.8304 MHz crystal controlled oscillator, divided to 4.9152 or 2.4576 MHz

RCA CMOS Microboard Computer
CDP18S600

Microboard Bus Interface Signals (Connector P1)

The following signals are generated or received by the CDP18S600 CPU Microboard and provide the interface to other Microboard Systems components. For further information on these signals, refer to the data sheet for the CDP1805A (File No. 1370). For a list of the pins and signals for the RCA Microboard Universal Backplane Connector (P1) as used on the CDP18S600, see Table 1.

DB7 through DB0 — Eight bidirectional data bus lines. Taken directly from the CPU bus pins, these lines transfer data among the memory, CPU, and I/O devices.

N0, N1, N2 — Taken directly from the CPU pins, these lines indicate an I/O instruction is being executed. They are derived from the low-order three bits of the N register during an I/O instruction execution only. They are low (false) at all other times. These bits form the primary address identifying the I/O device. Direction of transfer, derived from N3 internal to the CPU, is presented on the $\overline{\text{MRD}}$ line. When high, $\overline{\text{MRD}}$ indicates data transfer from I/O to memory; when low, from memory to I/O.

$\overline{\text{EF1}}$, $\overline{\text{EF2}}$, $\overline{\text{EF3}}$, $\overline{\text{EF4}}$ — Taken directly to the CPU pins, these inputs can be tested by conditional branch instructions. They, along with INT, DMAI, and DMAO are pulled high (inactive) with resistors. EF1 and EF2, gated by the PIO group address, are used to test the ready state of I/O ports A and B. EF3 and EF4, gated by the UART group address, are used to test the UART interrupt output and the serial data input line. The EF lines may be used to identify the source of an interrupt to the CPU, or they may be used to indicate priority or status.

$\overline{\text{INT}}$ — Taken directly to the CPU pin, the interrupt line causes a transfer of control from the current program counter to register 1. Interrupts may be inhibited by software. If Interrupt Enable (IE) is set, recognition of $\overline{\text{INT}}$ results in completion of execution of the current instruction, followed by an S3 machine state during which designators X and P are stored in T. Then, X is set to 2, P is set to 1, and IE is reset to 0. The S3 state lasts one machine cycle (eight clocks), after which processing resumes with R1 as program counter.

Table I: Pin Terminals and Signals for the RCA Microboard Universal Backplane

Component Side				Wire Side			
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
1	DMAI-N	In	DMA Input Request	A	TPA-P	Out	System Timing Pulse 1
2	DMAO-N	In	DMA Output	B	TPB-P	Out	System Timing Pulse 2
3	RNU-P	In	Run Utility Request	C	DBO-P	In/Out	Data Bus
4	INT-N	In	Interrupt Request	D	DB1-P	In/Out	Data Bus
5	MRD-N	Out	Memory Read	E	DB2-P	In/Out	Data Bus
6	Q-P	Out	Programmed Output Latch	F	DB3-P	In/Out	Data Bus
7	SC0-P	Out	State Code	H	DB4-P	In/Out	Data Bus
8	SC1-P	Out	State Code	J	DB5-P	In/Out	Data Bus
9	CLEAR-N	In	Clear-Mode Request	K	DB6-P	In/Out	Data Bus
10	WAIT-N	In	Wait-Mode Request	L	DB7-P	In/Out	Data Bus
11	-5V/-15V	—	Auxiliary Power	M	A0-P	Out	Multiplexed Address Bus
12	SPARE	—	Not Assigned	N	A1-P	Out	Multiplexed Address Bus
13	CLOCK OUT	Out	Clock from CPU Osc.	P	A2-P	Out	Multiplexed Address Bus
14	N0-P	Out	I/O Primary Address	R	A3-P	Out	Multiplexed Address Bus
15	N1-P	Out	I/O Primary Address	S	A4-P	Out	Multiplexed Address Bus
16	N2-P	Out	I/O Primary Address	T	A5-P	Out	Multiplexed Address Bus
17	EF1-N	In	External Flag	U	A6-P	Out	Multiplexed Address Bus
18	EF2-N	In	External Flag	V	A7-P	Out	Multiplexed Address Bus
19	EF3-N	In	External Flag	W	MWR-N	Out	Memory Write Pulse
20	+10V/+15V	—	Auxiliary Power	X	EF4-N	In	External Flag
21	+5V	—	+5 V dc	Y	+5V	—	+5V dc
22	GND	—	Digital Ground	Z	GND	—	Digital Ground

Note: Signal flow direction is relative to CPU.

Interrupts can result from an external source or from the counter/timer. Each can be separately enabled with XIE or CIE instructions

$\overline{\text{DMAI}}$, $\overline{\text{DMAO}}$ — Taken directly to CPU pins and not utilized by the CDP18S600, these lines allow off-board I/O controllers rapid direct memory access. The CPU monitors these data transfers, going into an S2 machine state for each byte transfer. R0 is used as the memory pointer and is automatically incremented each time. Thus, DMA transfers are interleaved with normal processing and no software action is required except to initialize R0 before transfer starts. INT and/or an EF may be used to notify the program that a block DMA transfer is completed so that initialization and processing of the data block may be performed. The DMA inputs may be maintained in the true state for contiguous S2 states for the most rapid transfer. In the usual case, however, the DMA request is removed at the TPA of the S2 cycle to obtain a single byte transfer, allowing time for normal processing and for setting up the next byte in the requesting controller. Each S2 state is eight clock cycles in duration.

SC1, SC0 — State code outputs from the CPU which identify the type of machine cycle in progress.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

TPA, TPB — Timing pulses generated by the CPU which occur once in each machine cycle. TPA trailing edge is used to latch the high-order memory address. TPB trailing edge is used to latch output data from the data bus.

All I/O cycles should be considered to start at the trailing edge of TPA and end at the trailing edge of TPB. MRD, the N lines, and the A7 through A0 lines are stable during this period. (To provide additional hold time on these lines, the CDP18S600 board latches them at TPB trailing edge, and holds them through the next leading edge of TPA.)

A7 through A0 — Eight memory address lines from the CPU. The 16 memory address bits are multiplexed on this address bus. The high-order eight bits are presented early in each machine cycle and must be latched at the TPA trailing edge. The CDP18S600 buffers, latches, and decodes these bits for the on-board memories. Any external memory must provide its own latches. During the latter part of the cycle, the low-order eight bits are presented on this address bus and need not be latched.

$\overline{\text{MWR}}$ — A WRITE command from the CPU to the memories. Address lines are stable at this time. Actual writing or latching occurs at the trailing edge.

$\overline{\text{MRD}}$ — A READ command from the CPU to the memories and a direction indicator for I/O data transfers. In the I/O instructions it corresponds to N3 (N register, internal to the CPU) which distinguishes I/O inputs from outputs. $\overline{\text{MRD}}$ must be used to condition output drivers in all memory components, or their output buffers, to avoid contention on the data bus. The absence of MWR must not be interpreted as a READ. Early in a write cycle, data are being driven onto the data bus by the CPU or an input device. If a memory allows its outputs to be enabled while $\overline{\text{MRD}}$ is false before MWR appears, bus contention will occur resulting in unnecessary power dissipation and perhaps circuit failures.

Q — A single bit output from the CPU. This bit is set or reset by SEQ (7B) or REQ (7A) instructions, and is also reset by CLEAR. It is available both on the Micro-board Bus (P1) and on the Parallel I/O connector (P2). Q may also be tested with a branch instruction, or may be toggled from the Counter/Timer.

CLOCK OUT — A 4.9152 or 2.4576 MHz square wave clock provided for general use. It is derived from the 9.8304 MHz on-board crystal controlled oscillator.

$\overline{\text{WAIT}}$, $\overline{\text{CLEAR}}$ — Two control inputs to the CPU which determine the mode of operation.

$\overline{\text{CLEAR}}$	$\overline{\text{WAIT}}$	MODE
L	L	Not allowed
L	H	Reset
H	L	Pause
H	H	Run

The functions of the modes are defined as follows:

RESET: Registers I, N, Q, counter prescaler, and counter interrupt (CI) are reset. IE, XIE, and CIE are set and 0's (Vss) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The state of the counter/timer is unaffected by the RESET operation.

The first machine cycle after termination of reset is an initialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1, X, P→T, and then registers X, P, and R(0) are reset. Interrupt and DMA

servicing are suppressed during the initialization cycle. The next cycle is an S0 or an S2 but never an S1 or S3. In most cases, it is desirable to reset the IE before starting processing. The use of a 71 instruction followed by 00 at memory locations 0000 and 0001 will reset IE which may be set later when the software is able to process interrupt. Power-up reset-run is provided on the CDP18S600 board.

PAUSE: Stops the internal CPU timing generator, freezing the state of the processor. Pause can occur at two points in a machine cycle, on the low-to-high transition of either TPA or TPB. The oscillator continues to run but subsequent clock transitions are ignored (see Fig. 2).

If Pause is entered while in the event counter mode, the appropriate E Flag transitions will continue to decrement the counter.

RUN: May be initiated from the Pause or Reset mode functions. If initiated from Pause, the CPU resumes operation at the point it left off. If paused at TPA, it will resume on the first high-to-low clock transition. If paused at TPB, it will resume on the first low-to-high clock transition (see Fig. 2). When run is initiated from the Reset operation, the first machine cycle following Reset is always the initialization clycle.

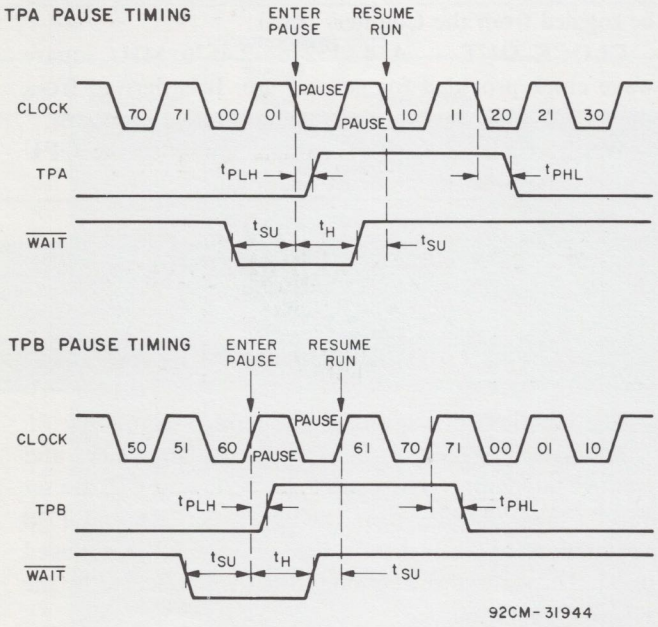

Fig. 2 - Pause mode timing waveforms.

The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

RNU — Run Utility Software. A signal supplied to CDP18S600 to force the most significant address true. As a result, the program start is at memory location 8000 instead of 0000. See discussion under Run Utility.

Counter-Timer and Controls

The CDP1805A provides an on-chip 8-bit presettable timer-counter. Software control of the counter allows the clock input to be TPA ÷ 32, EF1, EF2, TPA•EF1, or TPA•EF2, in addition to the Decrement-Counter Instruction.

The counter-timer logic shown in Fig. 3 consists of a presettable 8-bit down-counter (Modulo N type), and a conditional divide-by-32 prescaler. After counting down to $(01)_{16}$ the counter returns to its initial value at the next count and sets the Timer/Counter Interrupt. It will continue decrementing on subsequent counts. If the counter is preset to $(00)_{16}$ a full 256 counts will occur.

During a Load Counter instruction (LDC) if the counter was stopped with a STPC instruction, the counter and its holding register (CH) are loaded with the value in the D register and any previous counter interrupt is cleared. If the LDC is executed when the counter is running, the contents of the D register are loaded into the holding register (CH) only and any previous counter interrupt is not cleared. After counting down to $(01)_{16}$ the next count will load the new initial value into the counter, set the Counter Interrupt Latch, and operation will continue.

The timer/counter has the following five programmable modes:

1. **Event Counter 1:** Input to counter is connected to the $\overline{EF1}$ terminal. The high-to-low transition decrements the counter.
2. **Event Counter 2:** Input to counter is connected to the $\overline{EF2}$ terminal. The high-to-low transition decrements the counter.
3. **Timer:** Input to counter is from the divide-by-32 prescaler clocked by TPA. The prescaler is decremented on the low-to-high transition of TPA. The divide-by-32 prescaler is reset when the counter is in a mode other than the Timer mode or stopped by a STPC.
4. **Pulse Duration Measurement 1:** Input to counter connected to TPA. Each low-to-high transition of TPA decrements the counter if the input signal at $\overline{EF1}$ terminal (gate input) is low. On the transition of $\overline{EF1}$ to the positive state, the count is stopped, the mode is cleared, and the interrupt request latched. If the counter underflows while the input is low, interrupt will also be set, but counting will continue.

5. **Pulse Duration Measurement 2:** Operation is identical to Pulse Duration Measurement 1, except $\overline{EF2}$ is used as the gate input.

The modes can be changed without affecting the stored count.

Those modes which use $\overline{EF1}$ and $\overline{EF2}$ terminals as inputs do not exclude testing these flags for branch instructions.

The Stop Counter (STPC) instruction clears the counter mode and stops counting. The STPC instruction should be executed prior to a GEC instruction, if the counter is in the Event Counter Mode 1 or 2.

In addition to the five programmable modes, the **Decrement Counter instruction (DTC)** enables the user to count in software. In order to avoid conflict with counting done in the other modes, the instruction should be used only after the mode has been cleared by a Stop Counter instruction.

The Enable Toggle Q instruction (ETQ) connects the Q-line flip-flop to the output of the counter, such that each time the counter decrements from 01 to its next value, the Q output changes state. This action is independent of the counter mode and the Interrupt Enable flip-flops. The Enable Toggle Q condition is cleared by an LDC with the timer/counter stopped, system Reset, or a BCI with C1=1.

On-Board Memory Addressing

All 1800 series processors use a multiplexed address bus: the high byte is output first to be latched with TPA trailing edge, then the low byte is output. The CDP-18S600 also latches the low byte and holds it through the next TPA leading edge. This gives more address hold time after the memory write pulse and TPB. (TPB trailing edge is often used to strobe I/O output data.)

The latched A0 through A10 are sent to each memory socket, while A13 through A15 are decoded for chip selects. A11 and A12 may be used either at the socket or for chip select decoding depending on memory size.

The CDP18S600 provides 2 independent memory "banks", one of 4 sockets and one of 1 socket. Each socket may contain ROM, EPROM, or RAM of 2K x 8, 4K x 8, or 8K x 8 size, the only restriction being that all the memories within one bank be the same size. In addition, each socket may be disabled entirely.

Note that in the following discussion of memory address setting, all links within a given link pack not specifically called out as closed must be removed. Permanent circuit damage could result otherwise. Refer to the Parts List for manufacturers' part no's for Links.

Selecting Memory Type

Each socket, U17 through U21, has an associated 6

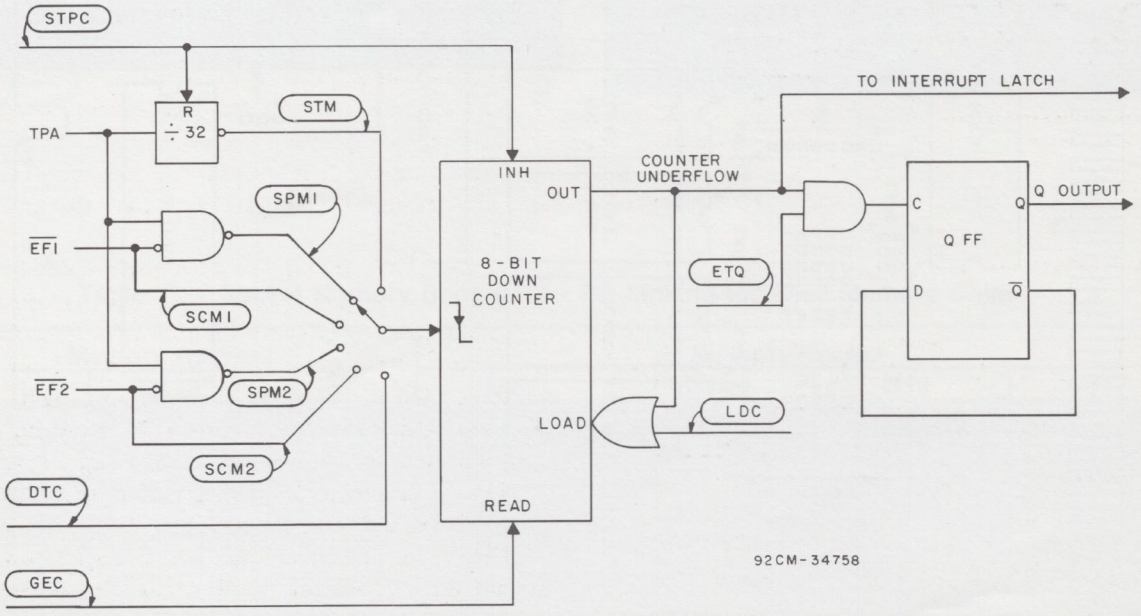

Fig. 3 - Timer/Counter diagram for CDP1805AC and CDP1806AC.

pin link pack, LK 6 through LK 10, used to set memory type. The link pack is found near pin 28 of each socket; see figure 4 for socket and link placement. Table II lists link connections needed for each memory type.

Table II: Links for setting memory type.

Generic Type	Size	Link
6116 RAM	2K x 8	1 - 2
6264 RAM	8K x 8	1 - 6, 2 - 3
2716 EPROM	2K x 8	2 - 5
2732 EPROM	4K x 8	2 - 3
2764 EPROM	8K x 8	2 - 3, 5 - 6

Note that EPROM's are Intel compatible pinout. Compatible ROM's could be substituted. Note also that a larger memory could be used to fill a smaller "hole," such as using a 6264 as a 4K RAM. Link the socket to fit the memory used, but link the decoder to provide the memory size desired as discussed below.

Note that all memory sockets are 28 pin. When using 24 pin memories, insert the chip so that pins 1, 2, 27, and 28 of the socket are left vacant. The chip should still be facing the same way as the socket.

Setting memory addresses: 1 socket memory bank (U21).

Link packs 11 and 14 (see Fig. 4) set the address of U21. Tables III, IV, and V give link pack 11 and 14 positions for 2K, 4K, and 8K x 8 memory sizes respectively.

Setting memory addresses: 4 socket memory bank (U20, 19, 18, 17)

Link pack 13 (see Fig. 3) sets the addresses of U20, 19, 18, and 17. Tables VI, VII, and VIII give link pack 13 positions for 2K, 4K, and 8K x 8 memory sizes respectively. Note that all link pack 12 links should also be made except when it is desired to disable a socket as discussed below.

Disabling memory sockets

As memory data lines are buffered, simply removing a memory chip will not free up that memory space. See Table IX for disabling each memory socket. As previously mentioned, link packs 6 through 10 are located near pin 28 of sockets U17 through 21.

To avoid floating inputs on the memory decoders, unused memory banks must still have a valid address setup on link packs 13 or 14.

When a socket is disabled, remove the contained memory chip.

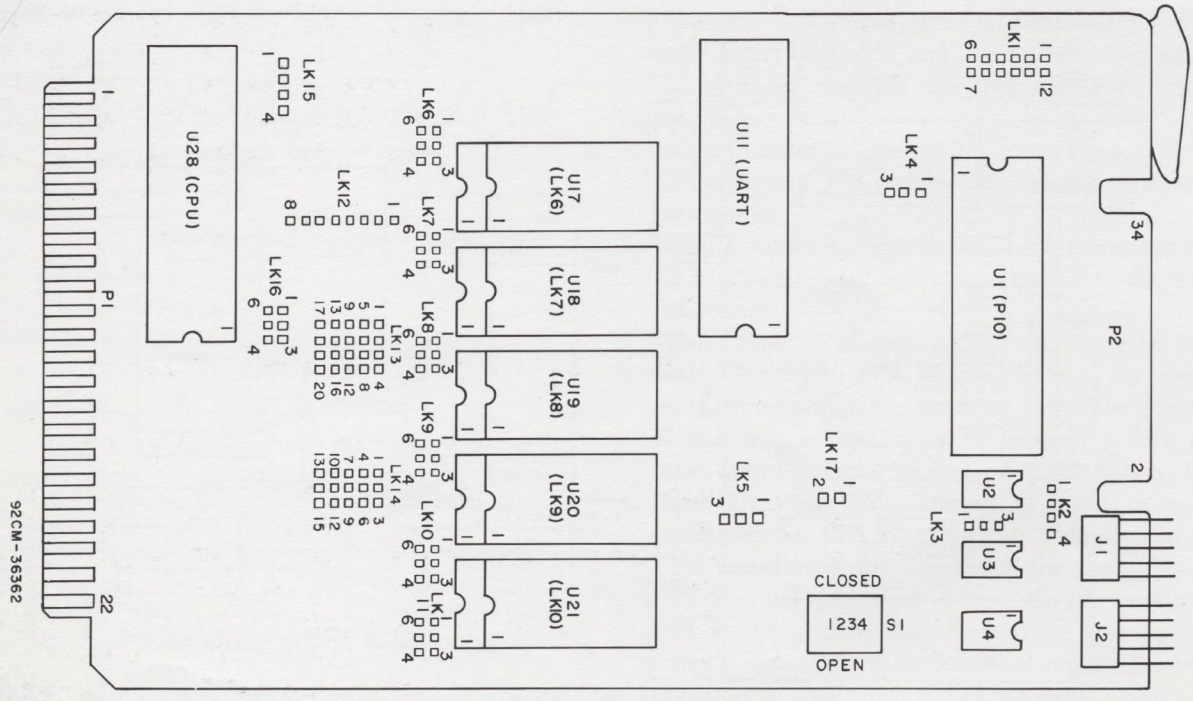

Fig. 4 - Links, Connectors, Baud Rate Switch, and Socketed I.C.s.

Table III: I Socket Memory Bank (U21) Linking for 2Kx8 Memory Chips

MEMORY ADDRESS		LK11			
	LK14	5 - 6	1 - 2	2 - 3	4 - 5
2 - 3, 5 - 6	7 - 8, 10 - 11, 13 - 14	0000 - 07FF	0800 - 0FFF	1000 - 17FF	1800 - 1FFF
	8 - 9, 10 - 11, 13 - 14	2000 - 27FF	2800 - 2FFF	3000 - 37FF	3800 - 3FFF
	7 - 8, 11 - 12, 13 - 14	4000 - 47FF	4800 - 4FFF	5000 - 57FF	5800 - 5FFF
	8 - 9, 11 - 12, 13 - 14	6000 - 67FF	6800 - 6FFF	7000 - 77FF	7800 - 7FFF
	7 - 8, 10 - 11, 14 - 15	8000 - 87FF	8800 - 8FFF	9000 - 97FF	9800 - 9FFF
	8 - 9, 10 - 11, 14 - 15	A000 - A7FF	A800 - AFFF	B000 - B7FF	B800 - BFFF
	7 - 8, 11 - 12, 14 - 15	C000 - C7FF	C800 - CFFF	D000 - D7FF	D800 - DFFF
	8 - 9, 11 - 12, 14 - 15	E000 - E7FF	E800 - EFFF	F000 - F7FF	F800 - FFFF

Table IV: I Socket Memory Bank (U21) Linking for 4Kx8 Memory Chips

Memory Address		LK11	
	LK14	5 - 6	2 - 3
1 - 2, 5 - 6	7 - 8, 10 - 11, 13 - 14	0000 - 0FFF	1000 - 1FFF
	8 - 9, 10 - 11, 13 - 14	2000 - 2FFF	3000 - 3FFF
	7 - 8, 11 - 12, 13 - 14	4000 - 4FFF	5000 - 5FFF
	8 - 9, 11 - 12, 13 - 14	6000 - 6FFF	7000 - 7FFF
	7 - 8, 10 - 11, 14 - 15	8000 - 8FFF	9000 - 9FFF
	8 - 9, 10 - 11, 14 - 15	A000 - AFFF	B000 - BFFF
	7 - 8, 11 - 12, 14 - 15	C000 - CFFF	D000 - DFFF
	8 - 9, 11 - 12, 14 - 15	E000 - EFFF	F000 - FFFF

Table V: I Socket Memory Bank (U21) Linking for 8Kx8 Memory Chips

Memory Address		LK11
	LK14	5 - 6
1 - 2, 4 - 5	7 - 8, 10 - 11, 13 - 14	0000 - 1FFF
	8 - 9, 10 - 11, 13 - 14	2000 - 3FFF
	7 - 8, 11 - 12, 13 - 14	4000 - 5FFF
	8 - 9, 11 - 12, 13 - 14	6000 - 7FFF
	7 - 8, 10 - 11, 14 - 15	8000 - 9FFF
	8 - 9, 10 - 11, 14 - 15	A000 - BFFF
	7 - 8, 11 - 12, 14 - 15	C000 - DFFF
	8 - 9, 11 - 12, 14 - 15	E000 - FFFF

Table VI: 4 Socket Memory Bank (U17 - 20) Linking for 2Kx8 Memory Chips

Memory Address		Memory Socket			
	LK13	U20	U19	U18	U17
1 - 2, 6 - 7	10 - 11, 14 - 15, 18 - 19	0000 - 07FF	0800 - 0FFF	1000 - 17FF	1800 - 1FFF
	11 - 12, 14 - 15, 18 - 19	2000 - 27FF	2800 - 2FFF	3000 - 37FF	3800 - 3FFF
	10 - 11, 15 - 16, 18 - 19	4000 - 47FF	4800 - 4FFF	5000 - 57FF	5800 - 5FFF
	11 - 12, 15 - 16, 18 - 19	6000 - 67FF	6800 - 6FFF	7000 - 77FF	7800 - 7FFF
	10 - 11, 14 - 15, 19 - 20	8000 - 87FF	8800 - 8FFF	9000 - 97FF	9800 - 9FFF
	11 - 12, 14 - 15, 19 - 20	A000 - A7FF	A800 - AFFF	B000 - B7FF	B800 - BFFF
	10 - 11, 15 - 16, 19 - 20	C000 - C7FF	C800 - CFFF	D000 - D7FF	D800 - DFFF
	11 - 12, 15 - 16, 19 - 20	E000 - E7FF	E800 - EFFF	F000 - F7FF	F800 - FFFF

Table VII: 4 Socket Memory Bank (U17 - 20) Linking for 4Kx8 Memory Chips

Memory Address LK13		Memory Socket U20	U19	U18	U17
2 - 6, 3 - 7, 5 - 9	14 - 15, 18 - 19	0000 - 0FFF	1000 - 1FFF	2000 - 2FFF	3000 - 3FFF
	15 - 16, 18 - 19	4000 - 4FFF	5000 - 5FFF	6000 - 6FFF	7000 - 7FFF
	14 - 15, 19 - 20	8000 - 8FFF	9000 - 9FFF	A000 - AFFF	B000 - BFFF
	15 - 16, 19 - 20	C000 - CFFF	D000 - DFFF	E000 - EFFF	F000 - FFFF

Table VIII: 4 Socket Memory Bank (U17 - 20) Linking for 8Kx8 Memory Chips

Memory Address LK13		Memory Socket U20	U19	U18	U17
2 - 3, 7 - 8, 5 - 9, 13 - 17	18 - 19	0000 - 1FFF	2000 - 3FFF	4000 - 5FFF	6000 - 7FFF
	19 - 20	8000 - 9FFF	A000 - BFFF	C000 - DFFF	E000 - FFFF

Table IX: Disabling memory sockets

Disabled socket	Remove links	Add links
U21	LK 10 and LK 11: all	LK 10: 4 - 5
U20	LK 9: all, LK 12: 1 - 2	LK 9: 4 - 5
U19	LK 8: all, LK 12: 3 - 4	LK 8: 4 - 5
U18	LK 7: all, LK 12: 5 - 6	LK 7: 4 - 5
U17	LK 6: all, LK 12: 7 - 8	LK 6: 4 - 5

Input/Output Interfacing

2 Level Addressing

In order to expand the number of I/O addresses available on RCA CDP1800 series mircoprocessors, a 2 level addressing scheme has been adopted on RCA Microboards. The data output during an "OUT 1" (61) instruction is latched by all I/O type Microboards. (This is referred to as a group select or 2 level address.) Boards decode either the lower nibble (bits 0 - 3) in a linear (1 of 4) manner, or the upper nibble in a binary (1 of 16) manner. Each I/O board compares this group number to the number assigned to it, and if the group matches, it can then respond to subsequent output (62 - 67) or input (6A - 6F) instructions. ("INP 1" (69) is reserved to read back, where implemented, the last group select address. The CDP18S600 board does not provide this function.)

Both the serial I/O, a CDP1854A UART, and the parallel I/O, a CDP1851 PIO, are enabled by linear group select bits. The UART may occupy either group 1 or 2, while the PIO is fixed in group 8. LK4 sets the UART group address; see figure 4 for location. Table X gives the group select choices. Note that utility programs such as UT70 require the UART to be in group 1.

Table X: UART and PIO group addresses

LK4 links	Group	Binary Address
1 - 2	UART group 1	XXXX 0001
2 - 3	UART group 2	XXXX 0010
XXXXX	PIO group 8	XXXX 1000

Note: X = don't care

Serial I/O

The CDP1854A UART has 4 registers. Once the UART group has been enabled, the registers are addressable as in Table XI below.

Table XI: UART I/O register addresses

Out 2: Load transmitter holding register
Out 3: Load control register
Inp 2: Read receiver holding register
Inp 3: Read status register

The control register sets, among other things, the word length, even/odd parity, parity enable, and number of stop bits. RCA utility routines, such as contained in RCA Monitor Program CDP18SUT70, set conditions of no parity, 8 data bits, and 2 stop bits. This setup requires an Out 3 instruction with data of hex 1D. For more information on setting up the UART, refer to the data

sheet for the CDP1854A, file number 1193.

The status register (Inp 3) holds transmitter and receiver status information. When bit 7, transmitter holding register empty, is set, it indicates that it is okay to load another output character for transmission. When bit 0, data available, is set, it indicates that a full character has been received and may be read.

The Out 2 instruction outputs data to be transmitted, and the Inp 2 instruction reads data that has been received.

The UART has an interrupt output that can be programmed to respond to several different status conditions; again refer to file 1193. The interrupt signal can be presented to the CPU INT — N or EF3 — N lines through links on LK1. The SDI (serial data in) signal can be sampled on EF4 — N through a third link on LK1; this allows a break condition to be detected (EF4 False). This link must be in place for running MICRODOS or equivalent. See Table XII for LK1 connections and Fig. 4 for LK1 location.

Both EF lines are driven through open collector gates and are disabled by removing the UART group select. The INT line is also open collector, but is not controlled with group select. In a system with multiple interrupts, the source of an interrupt could be determined by enabling group selects until an active flag was found.

Table XII: LK1 Connections

LK1 link	Connects
1 - 12	PIO interrupts to INT — N
2 - 11	UART interrupt to INT — N
3 - 10	PIO ARDY line to EF1 — N
4 - 9	PIO BRDY line to EF2 — N
5 - 8	UART interrupt to EF3 — N
6 - 7	UART SDI line to EF4 — N

The UART circuitry provides clear to send (CTS) handshaking as well as serial data input and output (SDI and SDO). Transmitting is stopped if the external CTS input is low (high at the UART). When receiving, the CTS output is lowered in the middle of the first stop bit, and raised again approximately 1/2 of a bit time after the rceiver holding register is read. This allows synchronization of sender and receiver. See Table XIII to disable CTS input handshaking. If U2 has been removed, jumper its socket, pins 2 to 4.

Table XIII: Selecting Serial Interface

Interface	LK2 (CTS)	LK3 (SDI)
RS232	1 - 2	1 - 2
RS422, unterminated	none	none
RS422, terminated with 200 Ohms	3 - 4	3 - 4
Disable (CTS input only)	1 - 2, 3 - 4	—

The serial data and CTS lines may use RS232, RS422, or 0 - 5 volt CMOS signal levels. RS232 uses ± 5 to ±15 volt single ended signals, while RS422 uses differential 2 volt signal levels. RS422 is intended for transmitting over longer distances or at greater speeds. Note that in RS232 the data is inverted and CTS is active high.

J2 provides the RS232 interface connections; see Table XIV for pin functions, and Fig. 5 for pin placement. U4 is the RS232 driver, and requires auxiliary supplies as outlined in the specifications. For applications where 0 to 5 volt output levels are acceptable, U4 may be removed and pins 1 to 3 and 5 to 7 jumpered. U2 is both the RS232 and RS422 receiver; select interface type by linking LK2 and LK3 as per Table XIII. RS232 and RS422 interfaces cannot be hooked up simultaneously.

J1 provides the RS422 interface. U3 is the RS422 driver while again U2 serves as the receiver. Input signals can be terminated with 200 Ohms to provide matching for longer distance cable runs; see Table XIII. Also see Table XIII to disable CTS input handshaking. When connecting RS422 inputs, the corresponding LK2 or LK3 pin 1 to 2 jumper must be removed; the short could damage the driver.

Table XIV: J1 (RS422) And J2 (RS232) Pin Functions

Pin No.	J1	J2
1	- CTS Out	Ground
2	- Data Out	- Data In
3	KEY	- Data Out
4	- CTS In	Tied High
5	- Data In	KEY
6	+ Data In	Tied High
7	+ CTS In	+ CTS Out
8	Ground	Tied High
9	+ Data Out	+ CTS In
10	+ CTS Out	Ground

J1 also provides a CMOS level interface. This allows a

low power serial communications link, but with less noise immunity than either RS232 or RS422. Remove U2, U3, and U4. Using 0.3 inch jumpers, connect U2 socket pins 2 to 7 and 3 to 6, and U3 socket pins 2 to 7 and 3 to 6. Open all LK2 and LK3 pins. The former RS422 "+" signal pins now carry the interface, although CTS is active low. If CTS input handshaking is not desired, jumper U2 socket pins 2 to 4.

SW1 sets the BAUD rate over a range of 50 to 38,400 bits/second. See Table XV for a list of available BAUD rates and switch settings.

Parallel I/O

The parallel I/O interface (P2) consists of 20 lines from a CDP1851 programmable I/O port, the CPU Q output and 4 flag inputs, clear, all 3 system supplies, and ground. P2 mates with a 34 conductor, 0.100 inch pitch, card edge connector. (Not supplied: see parts list for appropriate connectors.) See Fig. 5 for orientation, and Table XVI for a list of pin functions.

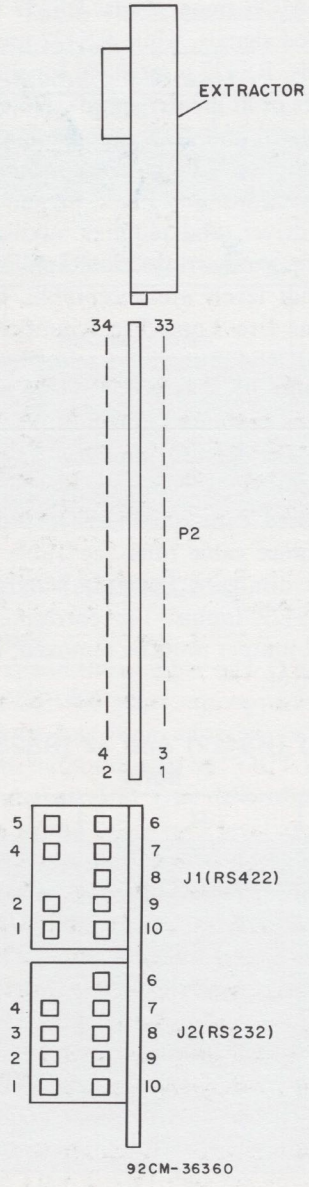

Fig. 5 - I/O Pin Positions - Edge View

Table XV: Baud Rate Selection Chart

Switch S1				Output Rate
4	3	2	1	Baud*
C	C	C	C	19200
C	C	C	O	38400
C	C	O	C	50
C	C	O	O	75
C	O	C	C	134.5
C	O	C	O	200
C	O	O	C	600
C	O	O	O	2400
O	C	C	C	9600
O	C	C	O	4800
O	C	O	C	1800
O	C	O	O	1200
O	O	C	C	2400
O	O	C	O	300
O	O	O	C	150
O	O	O	O	110

*Actual input to UART is 16 times the indicated output rate.
O=Open; C=Closed.

The RCA CDP1851 PIO consists of 2 - 8-bit ports, each with 2 handshaking lines, as well as internal control and status registers. The external ports (A and B) can be programmed as input or output, or one or both can be set in the bit-programmable mode. In this mode, each data and handshake line is a direction-programmable I/O line, and the PIO can generate interrupts on logical combinations of the data lines. Port A can also be placed in a bi-directional mode using all 4 handshake lines (requires port B to be in bit-programmable mode). Ports can be read back in the output mode, allowing a check of last byte output.

After first enabling the PIO group select as discussed previously, the CDP1851 registers may be addressed as in Table XVII. Note that the RCA Monitor Program

Table XVI: Microboard Computer Parallel I/O Connector (P2)

Pin	Signal	Pin	Signal
1	B2-P	2	GND
3	B1-P	4	B3-P
5	B0-P	6	B4-P
7	BSTB-P	8	B5-P
9	BRDY-P	10	B6-P
11	AD7-P	12	B7-P
13	AD6-P	14	GND
15	AD5-P	16	CLEAR-N
17	AD4-P	18	GND
19	AD3-P	20	Q-P
21	AD2-P	22	GND
23	AD1-P	24	EF4-N
25	AD0-P	26	EF3-N
27	ASTB-P	28	GND
29	ARDY-P	30	+ 5V
31	EF2-N	32	-5V/-15V
33	EF1-N	34	+10V/+15V

CDP18SUT70 also uses group 8 for enabling the CDP-18S651 floppy disk controller. The addresses within the group do not overlap, however, so this board may be operated with the CDP18SUT70 and the CDP18S651. (Software written to run on previous CPU cards such as the CDP18S601 will require shuffling of the PIO addresses.)

Table XVII: CDP1851 I/O Functions

I/O Instruction	CDP1851 Function
OUT 2 (62)	Write to port B
OUT 3 (63)	Write to port A
OUT 6 (66)	Write to Control Register
INP 2 (6A)	Read port B
INP 3 (6B)	Read port A
INP 6 (6E)	Read Status Register

Two of the handshake lines, ARDY and BRDY, can be linked to EF1 and EF2 respectively through open collector drivers. These are enabled with the PIO group select, and present active (low) flags if ARDY or BRDY are low. The two open collector interrupt lines from the PIO are tied together and may be linked to the CPU interrupt line. These are not conditioned with group select. Table XII gives linking. The use of the handshake and interrupt lines will be discussed under each mode of operation.

Setting Modes: The different modes of the PIO can be set by doing an OUT 6 with the data contained in Table XVIII. Note that modes should be set in the order shown; don't set port B as bit programmable then try to set port A as output. Also note that only port A can be bidirectional, and if set so, port B has to be bit programmable.

Table XVIII: Mode set and interrupt enable control words (OUT 6)

	PORT A	PORT B	BOTH PORTS
Input	0B	13	1B
Output	4B	53	5B
Bit-Programmable	CB*	D3*	DB*
Bi-Directional	8D	—	—
Enable Interrupts	81	89	—
Disable Interrupts	01	09	—

*Note: When Bit-Programmable mode is set, a second OUT 6 must follow with data to set bit direction: see text.

Enabling Interrupts: In the following mode discussions, interrupts can be used for a variety of handshaking chores or can result from a programmable logical function of input or output bits. To enable or disable interrupts, the data contained in Table XVIII must be written to the control register (OUT 6). This shouldn't be done until all other setup is accomplished. Reset disables all interrupts. Note that when interrupts are disabled, neither the open collector interrupt drivers nor the interrup bits in the status register can be active.

Input Mode: The input mode is entered either from reset or by setting it as in Table XVIII. If ASTB or BSTB is high (pulled high by on-board 10 KOhm resistors), then input data can be read continuously. If handshaking is desired, strobing ASTB or BSTB high then low will latch data into port A or B. The leading edge of the strobe will knock down ARDY or BRDY; these signals can then be used to signify "not ready for more data." The trailing edge of the strobe will set the PIO interrupt, if enabled, signalling the CPU to read the data. The leading edge of reading the PIO (INP 3 for port A, INP 2 for port B) will drop the interrupt request from that port, and the trailing edge will set ARDY or BRDY high again.

Since A and B interrupt drivers are tied together, the source must be determined by reading the status register (INP 6 — see Table XIX) or EF1 or 2. Status register bit

1 set or EF1 active indicates port A, while bit 0 or EF2 indicates port B. In a non-interrupt driven system, the status bits alone can be used for determining when data is available. Avoid using the flag lines alone unless the strobe pulse is known to be very narrow.

Note that on first entering the input mode, the ARDY and BRDY lines may be low; doing a "dummy" read will set them high. Also note that the STB, RDY, and all data lines have 10 KOhm pullup resistors.

Output Mode: When data is loaded into ports A or B (OUT 3 or 2), the ARDY or BRDY lines go high signifying "data available." The PIO interrupt goes inactive (if the other port isn't interrupting) as well as the EF1 or EF2 line. An external device accepting the data should respond by strobing ASTB or BSTB high then low. The strobe leading edge will knock down the ARDY or BRDY lines (EF1 or 2 go inactive), and the trailing edge will set the interrupt request. This signifies "data accepted, ready for more." (Output data can be read back if ASTB or BSTB is high.)

The same methods and precautions as described under input mode should be used for determining interrupt source.

Bit-Programmable Mode: The bit-programmable mode is entered by loading the control register (OUT 6) with the appropriate word from Table XVIII **A SECOND LOAD TO THE CONTROL REGISTER MUST FOLLOW** with data to program the direction of each bit. Every 0 in the byte will assign that bit position as an input, a 1 as an output. If both ports were set at once (OUT 6, data = hex DB), the second load will set the direction of both ports simultaneously.

Once a port is in the bit-programmable mode, its STB and RDY lines can also be programmed as input or output data lines. (Except when port A is bi-directional; BSTB and BRDY are assigned to it). Table XX gives the control register (OUT 6) bits for setting STB and RDY line use. Bit 1 selects which port is to be acted on. Bit 2 high allows bit 6 to set the RDY line direction, while bit 3 high allows bit 7 to set the STB line direction.

All STB and RDY lines can be read on the status register (INP 6), regardless of programmed direction. See Table XIX.

If STB or RDY are output bits, they can be written with an OUT 6. Bit 1 selects port A or B, bits 4 and 5 are the RDY and STB output data, and the remaining bits are 0's.

Note that ARDY and BRDY are outputs when reset is applied. If connected as inputs, that is to some other driving source, at least 1000 Ohms should be placed in series. This prevents damage by excessive current flow between the RDY output and the external source when reset is applied.

In the bit-programmable mode, the CDP1851 can generate interrupts on logical combinations of input or output bits. Table XXI gives the interrupt control word (OUT 6) bit assignments. Bit 3 selects port A or B, bit 4 indicates if a new interrupt mask is to follow, and bits 5 and 6 select the applicable logic function. When bit 4 is set, **A SECOND LOAD TO THE CONTROL REGISTER (OUT 6) MUST FOLLOW.** Every bit in the mask that is a 0 feeds the corresponding bit position in the port to the interrupt logic. A mask of hex FF is not allowed.

Once interrupt conditions are set up, interrupts have to be enabled by loading the appropriate control word from Table XVIII. The CPU interrupt signal and/or bits 0 and 1 from the status register can then monitor the logical conditions of the unmasked data bits.

Bidirectional Mode: Only port A can be bidirectional, and only if port B is first placed in the bit-programmable mode. Port A now uses all 4 handshake lines. Table XVIII gives the appropriate control word.

The ASTB and ARDY lines function for input handshaking the same as in the input mode. BSTB and BRDY function as output handshaking, the same as in the output mode, with the addition of BSTB being a 3-state control. With BSTB high, the port A output drivers

Table XIX: Status Register Bit Assignments (INP 6)

Bit-Programmable Mode Only				Bidirectional Mode Only		Any Mode	
Bit 7	6	5	4	3	2	1	0
BSTB Input Data	BRDY Input Data	ASTB Input Data	ARDY Input Data	A INT. Source = ASTB	A INT. Source = BSTB	A INT. Request	B INT Request

Table XX: STB and RDY Line Control Bit Assignments (Out 6)

Bit 7	6	5	4	3	2	1	0
STB Direction	RDY Direction	STB Output Data	RDY Output Data	Set STB Function	Set RDY Function	Port Select	0

0 = RDY = Input
1 = RDY = Output

0 = Select Port A
1 = Select Port B

0 = STB = Input
1 = STB = Output

0 = Don't Change RDY Function
1 = Set RDY Direction as Bit 6

0 = Don't Change STB Function
1 = Set STB Direction as Bit 7

are enabled.

Interrupts and CPU handshaking are the same as if both ports A and B were in use, except only the A interrupt request (status register bit 6) is active. To determine whether an input or output operation caused the interrupt, status register bits 2 and 3 must be checked. See Table XIX.

Table XXI:
Interrupt Control Bit Assignments (Out 6)

Bit 7	6	5	4	3	2	1	0
0	Select Logic Function		Mask Follows	Port Select	1	0	1

0 = Select Port A
1 = Select Port B

0 = No Change to Mask
1 = Next Byte is Mask*

0 0 = Interrupt if Any Unmasked Bit is Low
0 1 = Interrupt if Any Unmasked Bit is High
1 0 = Interrupt if All Unmasked Bits are Low
1 1 = Interrupt if All Unmasked Bits are High

*Note: When Bit 4 is Set, a Second Out 6 Must Follow to Set Interrupt Mask: See Text

Setting Clock Speed

There are 2 selectable clock speeds. LK5, pins 1 to 2, sets 4.9152 MHz, and pins 2 to 3 sets 2.4576 MHz. The selected clock is buffered and available on pin 13 of the backplane.

Not all available Microboards will accept the higher CPU speed. Table XXII gives presently available boards capable of running at the higher speed. Consult RCA for up to date information.

Table XXII: RCA Microboards with 5 MHz Capability

Memory	I/O
CDP18S628 32/64K RAM/ROM	CDP18S641B UART
CDP18S630 8K RAM	CDP18S651 Floppy Disk Controller
CDP18S631 16K RAM	CDP18S655 Real Time Clock
CDP18S632 32K RAM	CDP18S650 Counter/ Timer

Selecting Alternate CPU's

Although supplied with a CDP1805A CPU, any presently available 1800 series CPU may be used. Link 15 pins 1 to 2 and Link 16 allows use of different CPU's, and allow enabling/disabling of internal memory on CDP1804's. See Table XXIII for setting Links 15 and 16. (LK15, pins 3 - 4 disables RNU.)

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Table XXIII: RCA CPU Selection

CPU	LK15	LK16
CDP1802, 1802A, 1802B	1 - 2	2 - 3, 4 - 5
CDP1805, 1805A, 1806, 1806A	—	2 - 3, 4 - 5
CDP1804A, no internal memory	—	2 - 3, 4 - 5
CDP1804A, with internal RAM/ROM	—	1 - 2, 5 - 6

Note that the RCA CDP1804A with internal memory enabled uses on-chip memory address decoders. The user must make sure that none of the CDP18S600 memory is linked for the same addresses.

Run Utility

The RNU (backplane pin 3) signal is "OR'ed" with address bit 15 for the on-board memory address decoding. RCA utility programs, such as CDP18SUT70, are located at address hex 8000, and can thus be entered from reset if RNU is held high.

RNU is pulled low through a resistor for systems not requiring this function. Noise immunity can be increased by tying RNU low with LK15, pins 3 - 4. Make sure LK15, pins 3 - 4, is open if an active RNU source such as the MS1M40 or CDP18S640A is present in the system.

Power-On Clear

An R - C integrator and a Schmitt trigger provide approximately a 180 MSec long CLEAR-N signal when the +5 volt supply is turned on. This open collector, active low signal appears on the backplane and the parallel interface connector, and is used to initialize the CPU, UART, and PIO. It also disables all memory chip selects, and the CPU, backplane and UART clocks. It does not reset the group select latch, nor stop the oscillator.

The CLEAR-N signal resets the UART interrupt flip-flop, receiver holding register, control and status registers, and sets SDO high (low at the RS232 interface). It also sets both PIO ports to input mode, resets the status register, drops both RDY lines, disables interrupts, and sets the interrupt mask register to all O's (all bits enabled). It does not reset data already loaded in the PIO.

The CPU clear function has been discussed under "Microboard Bus Interface Signals".

If an external power-up reset or reset/RUN U source is available, such as on the MSIM40 supply and control module, the on-board power-up clear should be disabled. Link LK17 pins 1 - 2.

Using On-Chip RAM

The 64 byte RAM contained in the CDP1805A CPU (or the CDP1804A when internal decoding is disabled) may be accessed through an external decoder. LK15 pin 2 is the low-active memory enable input. LK 11, pins 6, 1, 3, and 4 are 4 decoded active low chip selects. An unused pin could be jumpered to the CPU memory enable input. See Tables IV, V, or VI for the 1 socket memory bank decoding. (The 64 byte RAM will "wrap around" to fill the entire 2, 4, or 8K decoded space.

Installation in Microboard Systems

The CDP18S600 may be installed in the CDP18S008, MS2000, or CDP18S693, 694, or 695 development system, or in the CDP18S670 or MSI series of industrial chassis. It is intended for use only in systems with a Microboard Universal Backplane. See each system manual for appropriate memory address requirements. The CDP18S600 may be run at its higher clock speed in the RCA MS2000 Micro Disk Development System with the standard board complement, thus increasing throughput. **Use in other systems or with non-designated boards requires use of the lower clock speed.**

Linking Summary

Table XXIV: Summary of System Link Connections

Link	Use	Referenced From
LK1	PIO and UART: flags and interrupts	Table XII
LK2, 3	CTS, SDI: select RS232, RS422	Table XIII
LK4	Set UART group number	Table X
LK5	Set CPU clock speed	Setting Clock Speeds
LK 6 - 10	Set U17 — 21 memory types	Tables II, IX
LK11, 14	Set U21 memory address	Tables III, IV, V, IX
LK12, 13	Set U17 — 20 memory addresses	Tables VI, VII, VIII, IX
LK15	Set CPU type, disable RUN Utility	Table XXIII, Run Utility
LK16	Set CPU type, use	Table XXIII
LK17	Disable power-on clear	Power-On Clear

Parts List

C1, C2, C6, C9 - C15 = 0.1uf, ± 20%, 50V
C3, C4 = 2.2 uf ± 20%, 20V
C5 = 47 pf, ± 10%, 200V
C7 = 10 pF, ± 10%, 200V
C8 = 39 pF, ± 10%, 200V
C16 = 4.7 uF, ± 10%, 10V
CR1 = 1N914B Diode
R1 = 10 Meg, ¼W, 5%
R2 = 3K, ¼W, 5%
R3, R5 = 10K, ¼W, 5%
R4, R6 = 200 Ohm, ¼W, 5%
R7 = 2.2K, ¼W, 5%
R8 = 1.8 Meg, ¼W, 5%
N1 = 10K, 8-pin resis. network
N2, N4, N6 = 10K, 10-pin resis. network
N3 = 10K, 6-pin resis. network
N5 = 22K, 10-pin resis. network
Y1 = 9.8304 MHz crystal
S1 = pos. DIP switch
J1, J2 = 10-pin rt. angle connector
  Mates with:
    Header: AMP No. 1-86148-2
    Contacts: AMP No. 1-87309-4
    Keying Plug: AMP No. 87077-1
      (supplied)
U1 = CDP1851CE
U2 = 9637ARM EIA Reciever
U3 = 9638RM EIA Driver
U4 = CA3240E
U5, U6, U9 = CD40107BE
U7, U10 = CD74HC14E
U8, U25, U31 = CD74HC75E
U11 = CDP1854ACE
U12 = CD74HC164E
U13 = CD74HC74E
U14, U26 =CD74HC02E
U15 = 4702BPC Baud Rate Generator
U16 = CD74HC245E
U21 = HM6116IP-4 2Kx8 RAM
U22 = CD74HC27E
U23 = CD74HC11E
U24, U27 = CPD1866CE
U28 = CDP1805ACE
U29 = CD74HC4075E
U30 = CD74HC373E
U32 = CD74HC367E
Card Extractor - MSIA 11
XU1, XU11, XU28 = Socket, 40-pin
XU2, XU3, XU4 = Socket, 8-pin
XU17 - XU21 = Socket, 28-pin

P2 mates with a variety of 34-pin flat cable connectors such as T & B Ansley 609-3415M, Berg 65764-005, 3M 3463-0001, or equivalent (not supplied)

Push-on links:
  AMP No. 531220-3
  Berg 76264-101
    or equivalent

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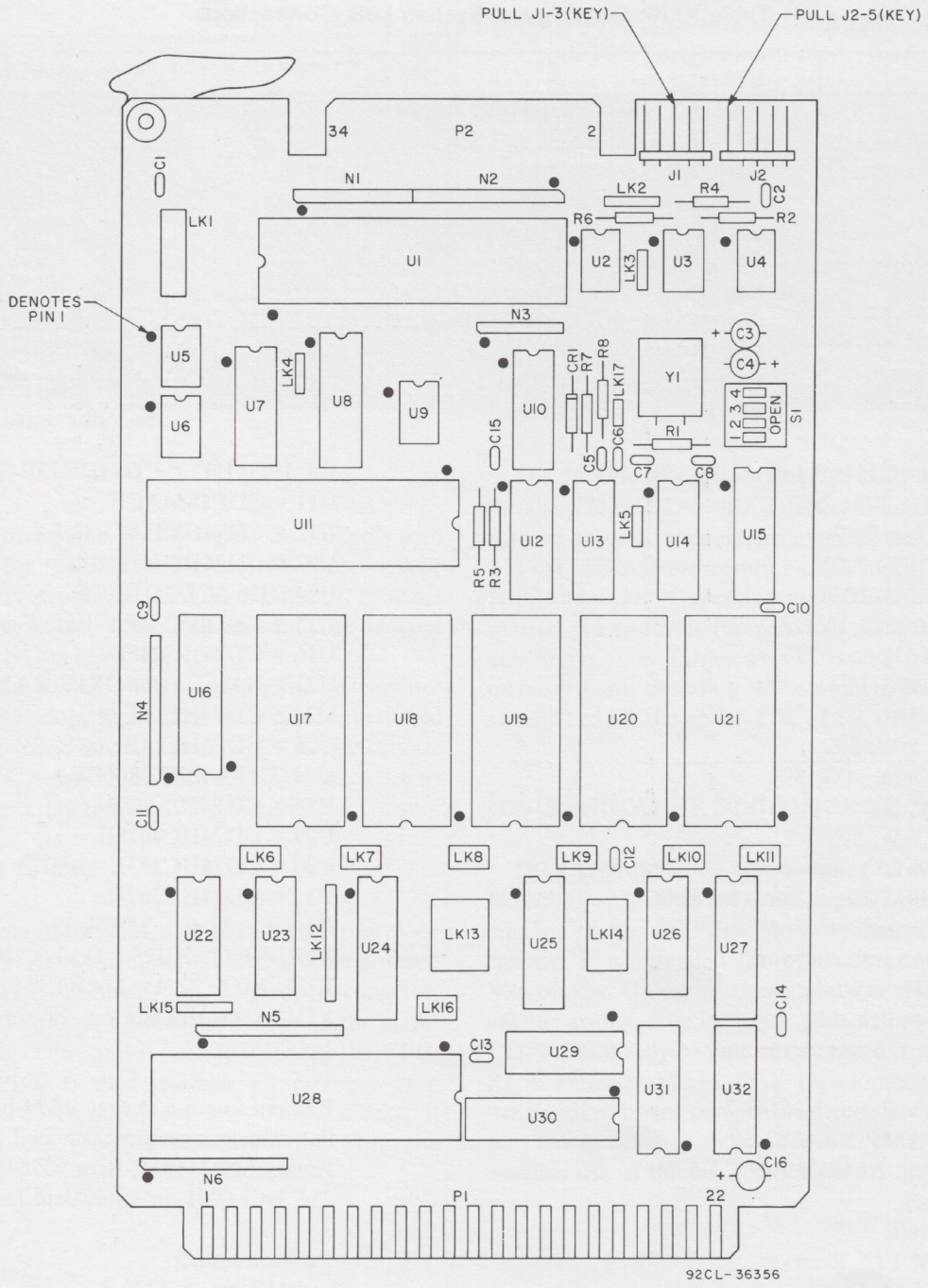

Fig. 6 - Microboard Computer CDP18S600 Layout Diagram.

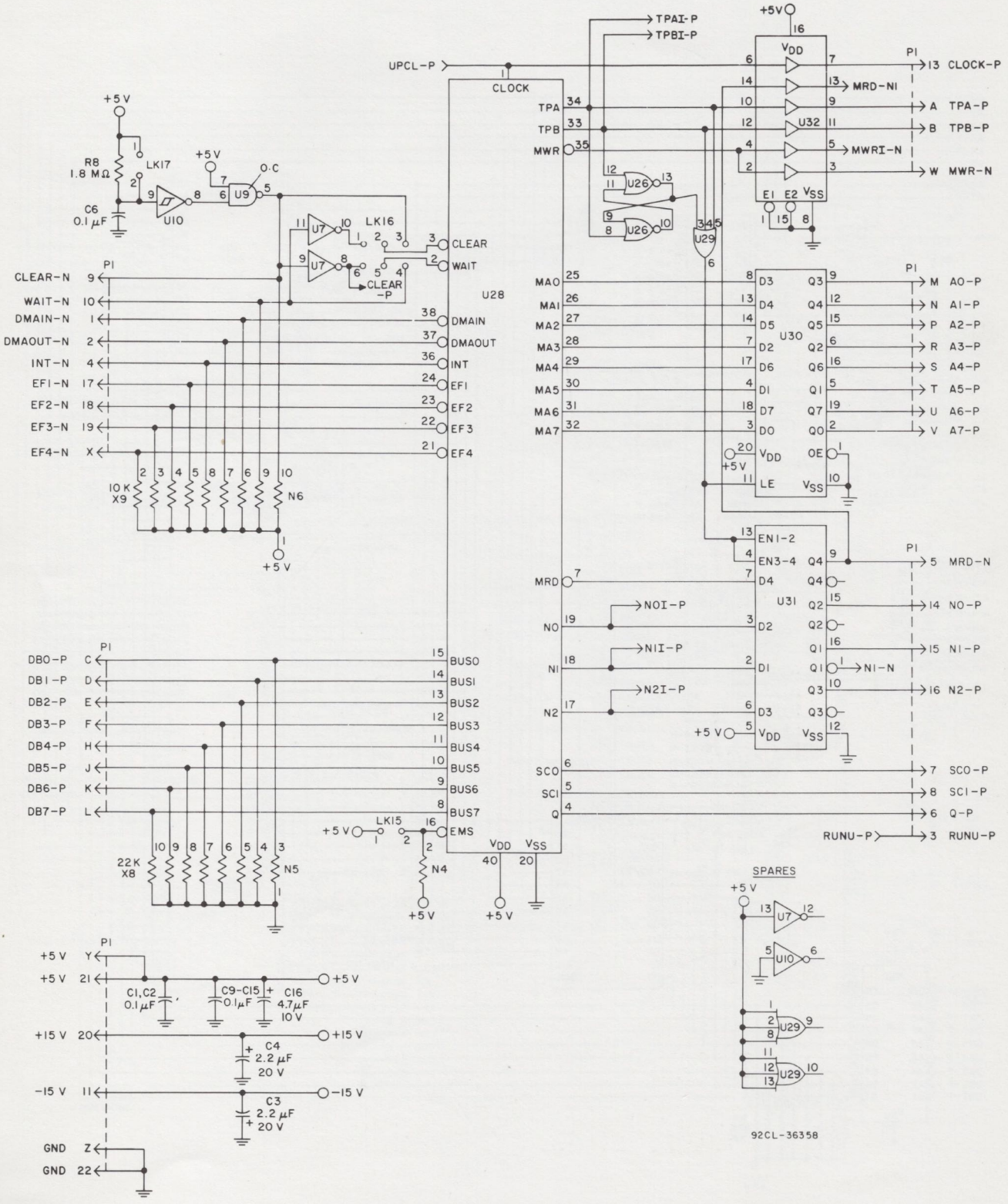

Fig. 7 - Microboard Computer CDP18S600 Logic and Circuit Diagram - Central Processor Unit.

RCA CMOS Microboard Computer

CDP18S600

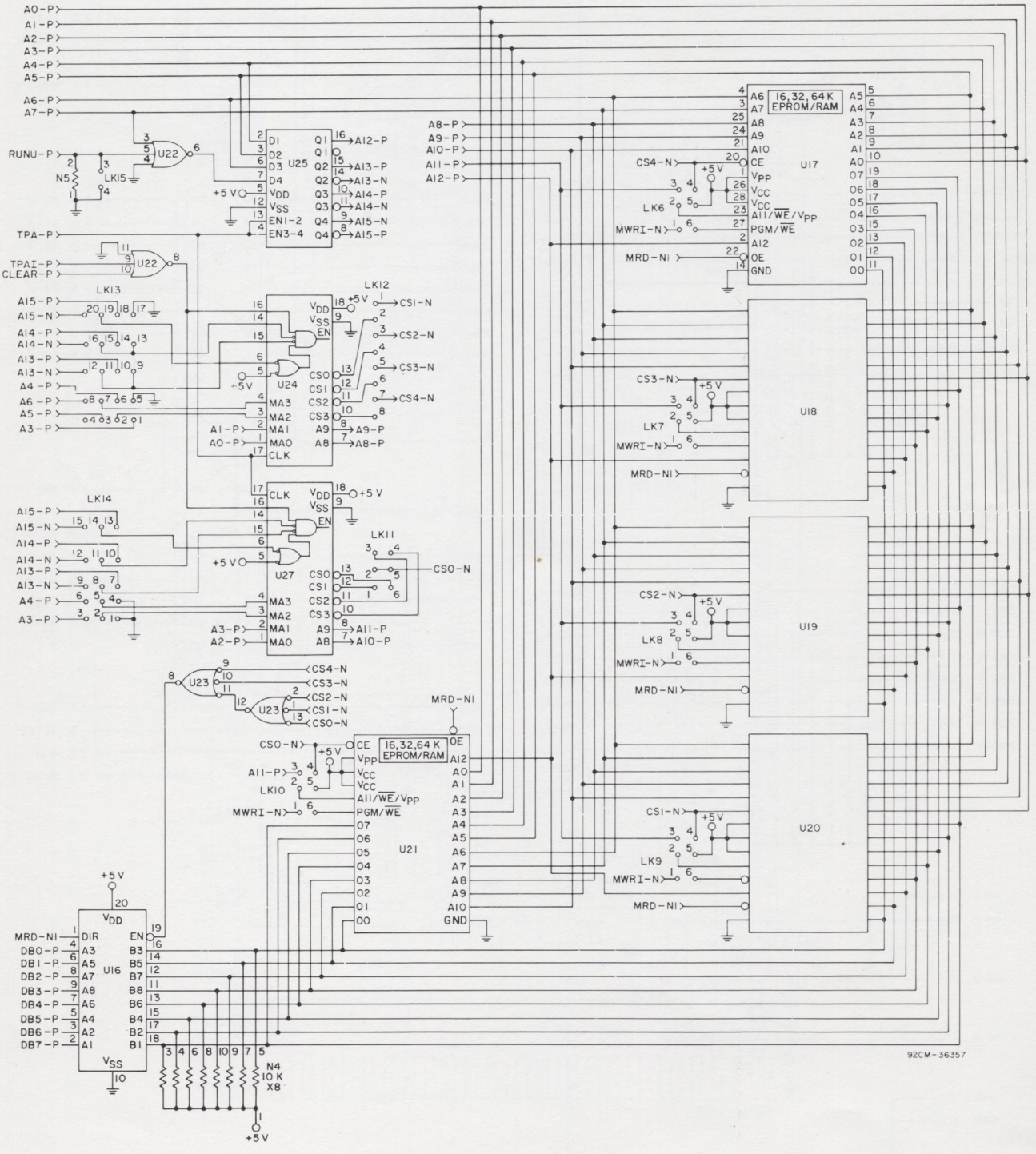

Fig. 8 - Microboard Computer CDP18S600 Logic and Circuit Diagram - Memory Portion.

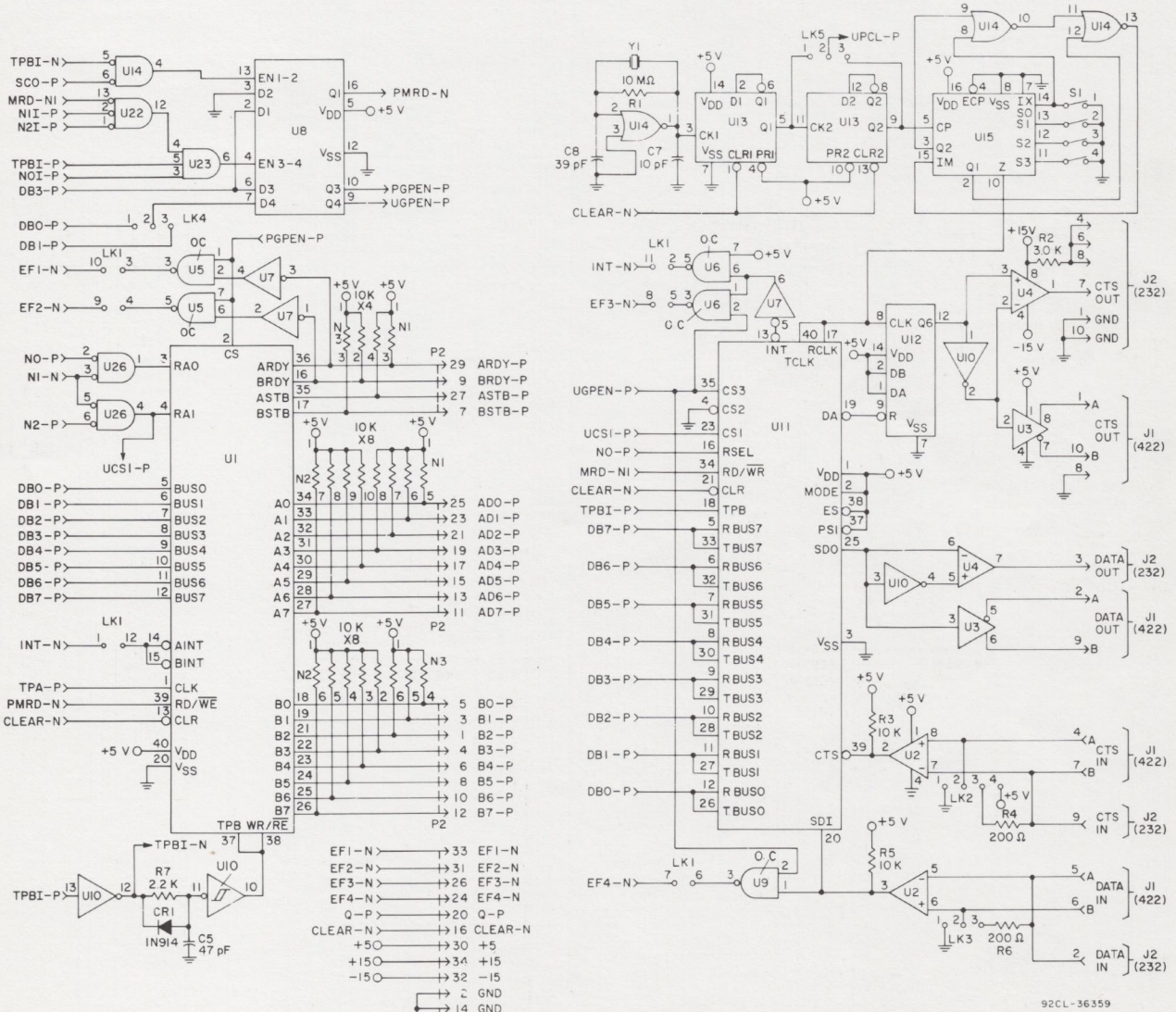

Fig. 9 - Microboard Computer CDP18S600 Logic and Circuit Diagram - I/O Portion.

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